CLAIMS

What is claimed is:

1. A method for identifying data sources associated with a circuit design, comprising:

retrieving data source information including identification of a data source used to generate data for an entity in a design portion of interest in the circuit design;

formatting the data source information as a bit vector associated with the entity, wherein each of a plurality of bits in the bit vector comprises indicia applicable to the entity; and

processing the bit vector to generate formatted output.

2. The method of claim 1, wherein the entity is at least one design element in the design portion of interest.

3. The method of claim 1, wherein the entity is a group of design elements in the design portion of interest.

4. The method of claim 1, wherein the entity is an HLSN in the design portion of interest.

5. The method of claim 1, wherein the entity is a net in the design portion of interest.

6. The method of claim 1, wherein the indicia includes information that identifies at least one specific data source applicable to the entity.

7. The method of claim 1, wherein the step of retrieving further includes retrieving information that identifies a type of analysis performed by the CAD tool, and wherein the indicia identifies a specific type of the analysis.

8. The method of claim 1, wherein the step of retrieving includes retrieving data source information that identifies limits that were applied to numeric quantities in the analysis, and wherein the indicia identifies the limits.

9. The method of claim 1, wherein the step of retrieving includes retrieving data source information that identifies errors that occurred while processing a design element, and wherein the indicia identifies the errors.

10. The method of claim 1, further comprising displaying the bit vector.

11. The method of claim 1, further comprising storing the bit vector in a file.

12. The method of claim 1, wherein the bit vector is overloaded such that a specific subset of a plurality of bits therein has a significance dependent on the specific subset and on usage context of the bit vector.

13. The method of claim 1, wherein the indicia identifies a specific type of the analysis.

14. The method of claim 1, wherein the indicia identifies limits that were applied to numeric quantities in the analysis.

15. The method of claim 1, wherein the indicia identifies errors that occurred while processing a design element in the design portion of interest.

16. A system for identifying a data source used by a CAD tool in analysis of a circuit design, wherein a plurality of data sources are available to the CAD tool, comprising:

a processor coupled to a computer memory;

a plurality of data source indicators, stored in the computer memory, each of which comprises a plurality of bits for identifying the data sources associated with an entity in a design portion of interest in the circuit design; and

a table, stored in the computer memory, for formatting the data source indicators.

17. The system of claim 16, wherein the data source indicators are generated from information retrieved from the data sources.

18. The system of claim 16, wherein a plurality of the bit vectors are processed by the processor to generate formatted output.

19. A system for identifying data sources associated with a circuit design, comprising:

means for retrieving data source information that identifies at least one of the data sources;

means for formatting the data source information as a bit vector, wherein each of a plurality of bits in the bit vector comprises indicia of a specific data source applicable to an entity in a design portion of interest in the circuit design; and

means for processing the bit vector to generate formatted output.

20. A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for identifying data sources used in analysis of a circuit design, comprising:

instructions for retrieving data source information that identifies a data source;

instructions for formatting the data source information as a bit vector, wherein each of a plurality of bits in the bit vector comprises indicia of the data source applicable to an entity in a design portion of interest in the circuit design; and

instructions for processing the bit vector to generate formatted output.